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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,654	04/09/2001	Frank Preiss	00P7569US01/059001	9718

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EXAMINER	
HO, CHUONG T	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/829,654	PREISS ET AL.	
	Examiner	Art Unit	
	CHUONG T. HO	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/26/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-16 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sarkissian et al. (U.S.Patent No. 6,529,502 B2) in view of Ober (U.S.Patent No. 6,202,104 B1).

In the claim 1, see figure 3, Sarkissian et al. discloses a processor for in a Voice over Internet Protocol (VoIP) (see col. 11, line 35) telephone comprising:

- A bus (communications system 50 includes at least three separate types of buses, e.g., TDM bus 78, packet bus 80A (or 80B) or control bus 92) (see figure 3, col. 7, lines 50-62);
- A processor (79C DSP) core coupled to the bus (see figure 3);
- A packet handler (LAN BUS 81) coupled to the bus, the packet handler including plurality of first port for interfacing to one or more workstations (24) (see figure 3, col. 9, lines 32-35);
- A voice handler coupled to the bus, the voice handler including at least one second port for interface to a telephone (12) (see figure 3, col. 8, lines 60-67).

- A cell/frame handler (ATM 79B) coupled to the bus (78), the cell/frame handler adapted to couple to one or more packet networks (see figure 3, col. 9, lines 20-21);
- A peripheral control processor (DSP 76) coupled to the bus (84).

However, Sarkissina et al. is silent to disclosing a peripheral control processor to the bus for handling interrupts and DMA requests.

Ober (U.S.Patent No. 6,202,104 B1) discloses a peripheral control processor to the bus for handling interrupts and DMA requests (see figure 1, col. 2, lines 62-67).

Both Sarkissina and Ober discloses the peripheral control processor and buffer memory access. Ober recognizes a peripheral control processor to the bus for handling interrupts and DMA requests. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Sarkissina with the teaching of Ober to provide a peripheral control processor to the bus for handling interrupts and DMA requests in order to consumes power unnecessary.

3. In the claim 5, see figure 3, Sarkissian et al. discloses a processor for in a Voice over Internet Protocol (VoIP) (see col. 11, line 35) telephone comprising:

- A bus (communications system 50 includes at least three separate types of buses, e.g., TDM bus 78, packet bus 80A (or 80B) or control bus 92) (see figure 3, col. 7, lines 50-62);
- A processor (79C DSP) core coupled to the bus (see figure 3);

- A packet handler (LAN BUS 81) coupled to the bus, the packet handler including plurality of first port for interfacing to one or more workstations (24) (see figure 3, col. 9, lines 32-35);
- A voice handler coupled to the bus, the voice handler including at least one second port for interface to a telephone (12) (see figure 3, col. 8, lines 60-67).
- A cell/frame handler (ATM 79B) coupled to the bus (78), the cell/frame handler adapted to couple to one or more packet networks (see figure 3, col. 9, lines 20-21);
- A peripheral control processor (DSP 76) coupled to the bus (84).

However, Sarkissina et al. is silent to disclosing a peripheral control processor to the bus for handling interrupts and DMA requests.

Ober (U.S.Patent No. 6,202,104 B1) discloses a peripheral control processor to the bus for handling interrupts and DMA requests (see figure 1, col. 2, lines 62-67).

Both Sarkissina and Ober discloses the peripheral control processor and buffer memory access. Ober recognizes a peripheral control processor to the bus for handling interrupts and DMA requests. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Sarkissina with the teaching of Ober to provide a peripheral control processor to the bus for handling interrupts and DMA requests in order to consumes power unnecessary.

4. In the claim 9, see figure 3, Sarkissian et al. discloses a processor for in a Voice over Internet Protocol (VoIP) (see col. 11, line 35) telephone comprising:

A local area network (see col. 9, lines 33-35, lines 48-50);

A workstation (24, figure 3);

A Voice over Internet Protocol interface coupling the telephone (12) coupling the telephone and the workstation (24) to the local area network (see col. 9, lines 48-50), the VoIP interface including VoIP (see col. 11, line 24, 35) processor, the voice processor including:

- A bus (communications system 50 includes at least three separate types of buses, e.g., TDM bus 78, packet bus 80A (or 80B) or control bus 92) (see figure 3, col. 7, lines 50-62);
- A processor (79C DSP) core coupled to the bus (see figure 3);
- A packet handler (LAN BUS 81) coupled to the bus, the packet handler including plurality of first port for interfacing to one or more workstations (24) (see figure 3, col. 9, lines 32-35);
- A voice handler coupled to the bus, the voice handler including at least one second port for interface to a telephone (12) (see figure 3, col. 8, lines 60-67).
- A cell/frame handler (ATM 79B) coupled to the bus (78), the cell/frame handler adapted to couple to one or more packet networks (see figure 3, col. 9, lines 20-21);
- A peripheral control processor (DSP 76) coupled to the bus (84).

However, Sarkissina et al. is silent to disclosing a peripheral control processor to the bus for handling interrupts and DMA requests.

Ober (U.S.Patent No. 6,202,104 B1) discloses a peripheral control processor to the bus for handling interrupts and DMA requests (see figure 1, col. 2, lines 62-67).

Both Sarkissina and Ober discloses the peripheral control processor and buffer memory access. Ober recognizes a peripheral control processor to the bus for handling interrupts and DMA requests. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Sarkissina with the teaching of Ober to provide a peripheral control processor to the bus for handling interrupts and DMA requests in order to consumes power unnecessary.

5. In the claim 13, see figure 3, Sarkissian et al. discloses a processor for in a Voice over Internet Protocol (VoIP) (see col. 11, line 35) telephone comprising:

A local area network (see col. 9, lines 33-35, lines 48-50);

A workstation (24, figure 3);

A Voice over Internet Protocol interface coupling the telephone (12) coupling the telephone and the workstation (24) to the local area network (see col. 9, lines 48-50), the VoIP interface including VoIP (see col. 11, line 24, 35) processor, the voice processor including:

- A bus (communications system 50 includes at least three separate types of buses, e.g., TDM bus 78, packet bus 80A (or 80B) or control bus 92) (see figure 3, col. 7, lines 50-62);
- A processor (79C DSP) core coupled to the bus (see figure 3);
- A packet handler (LAN BUS 81) coupled to the bus, the packet handler including plurality of first port for interfacing to one or more workstations (24) (see figure 3, col. 9, lines 32-35);

- A voice handler coupled to the bus, the voice handler including at least one second port for interface to a telephone (12) (see figure 3, col. 8, lines 60-67).
- A cell/frame handler (ATM 79B) coupled to the bus (78), the cell/frame handler adapted to couple to one or more packet networks (see figure 3, col. 9, lines 20-21);
- A peripheral control processor (DSP 76) coupled to the bus (84).

However, Sarkissina et al. is silent to disclosing a peripheral control processor to the bus for handling interrupts and DMA requests.

Ober (U.S.Patent No. 6,202,104 B1) discloses a peripheral control processor to the bus for handling interrupts and DMA requests (see figure 1, col. 2, lines 62-67).

Both Sarkissina and Ober discloses the peripheral control processor and buffer memory access. Ober recognizes a peripheral control processor to the bus for handling interrupts and DMA requests. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Sarkissina with the teaching of Ober to provide a peripheral control processor to the bus for handling interrupts and DMA requests in order to consumes power unnecessary.

6. In the claims 2, 6, 10, 14, Sarkissina discloses the packet handler includes a bus bridge (LAN BUS) for interfacing to the bus, a 10/100b T interface, a wireless LAN interface, a Universal serial bus interface, and a home phoneline networking alliance interface (see col. 9, lines 32-50).

7. In the claims 3, 7, 11, 15, Sarkissina discloses the voice handler includes a bus bridge (TDM BUS) for interface to the bus, one or more PCM ports (POT), a mailbox, and DSP core (DSP 79C) (see col. 8, lines 60-67).

8. In the claims 4, 8, 12, 16, Sarkissina discloses the cell/frame handler (ATM 79B) includes a frame handler (ATM) for sending and receiving frames over the one or more packet networks (packet 1, packet 2) an ATM handler for sending and receiving data over ATM network, and an encryption unit for encrypting the data (see col. 11, lines 30-38).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571) 272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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